ABSTRACT

[00039] The loss of data and/or the corruption of data that may occur in flash memory when a reset signal is received during a memory write cycle is prevented by delaying reset signals sent to the flash memory for a time period sufficient for a write cycle to be completed. The loss of data and/or the corruption of data that may occur in flash memory when the power supply is interrupted during a write cycle is prevented by providing a DC-to-DC converter with one or more large capacitors in parallel with its input as the power supply to the flash memory. If the system power supply fails or is interrupted, the discharge of the capacitor(s) delays the voltage decay at the input of the DC-to-DC converter such that the output of the DC-to-DC converter remains within tolerance for a time sufficient for the flash memory to complete a write cycle.